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- 1 [Toward efficient and robust software speculative parallelization on m](#)  
 Marcelo Cintra, Diego R. Llanos  
 June 2003 **PPoPP '03: Proceedings of the ninth ACM SIGPLAN symposium on programming**

**Publisher:** ACM [Request Permissions](#)

 Full text available: [Pdf](#) (330.64 KB)

 Additional Information: [full citation](#), [abstract](#)
**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 101, Downloads

With speculative parallelization, code sections that cannot be fully analyzed are executed in parallel. Hardware schemes are fast but expensive and require a large memory system. Software schemes ...

**Keywords:** speculative parallelization, thread-level speculation

Also published in:

 October 2003 **SIGPLAN Notices** Volume 38 Issue 10

- 2 [Transient fault prediction based on anomalies in processor events](#)  
 Satish Narayanasamy, Ayse K. Coskun, Brad Calder  
 April 2007 **DATE '07: Proceedings of the conference on Design, automation and test in Europe**  
**Publisher:** EDA Consortium  
 Full text available: [Pdf](#) (173.56 KB)

 Additional Information: [full citation](#), [abstract](#)
**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 26, Downloads

Future microprocessors will be highly susceptible to transient errors as technology scales. Prior techniques advocated full scale structural or temporal redundancy, but they can provide ...

- 3 [Exploiting reference idempotency to reduce speculative storage overhead](#)  
 Seon Wook Kim, Chong-Liang Ooi, Rudolf Eigenmann, Babak Falsafi, T. N. S. Ravi  
 September 2006 **Transactions on Programming Languages and Systems**

**Publisher:** ACM [Request Permissions](#)



 Full text available: [Pdf](#) (433.96 KB)

 Additional Information: [full citation](#), [abstract](#)
**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 33, Downloads

Recent proposals for multithreaded architectures employ speculative execution to execute dependences speculatively in parallel. The architectures use


speculative data, track data dependences ...

**Keywords:** Idempotent references, compiler-assisted speculative execu




- 4 **Recovery code generation for general speculative optimizations**  
 Jin Lin, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin-Fook Ngai  
 March 2006 **Transactions on Architecture and Code Optimization (TACO)**  
**Publisher:** ACM  Request Permissions  
 Full text available:  Pdf (909.58 KB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 45, Download

A general framework that integrates both control and data speculation rules has shown to improve CPU2000 performance on Itanium systems. check instructions and ...

**Keywords:** Recovery code, multi-level data speculation, speculative SS

- 5 **A Compiler Framework for Recovery Code Generation in General Speculative Execution**  
 Jin Lin, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin-Fook Ngai  
 September 2004 **PACT '04: Proceedings of the 13th International Conference on Parallel Architectures and Compilation Techniques**  
**Publisher:** IEEE Computer Society  
 Full text available:  Pdf (186.86 KB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 17, Download

A general framework that integrates both control and data speculation rules has shown to improve SPEC2000 performance on Itanium systems. check instructions and ...




- 6 **Simultaneous speculative threading: a novel pipeline architecture in multi-processor systems**  
 Shailender Chaudhry, Robert Cypher, Magnus Ekman, Martin Karlsson, Andre Tremblay  
 June 2009 **ISCA '09: Proceedings of the 36th annual international symposium on Computer Architecture**  
**Publisher:** ACM  Request Permissions  
 Full text available:  Pdf (1.30 MB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 53, Downloads (12 Months): 749, Download

This paper presents Simultaneous Speculative Threading (SST), which is an area- and power-efficient cores for chip multiprocessors. SST hardware is derived from a single sequential ...

**Keywords:** checkpoint-based architecture, chip multiprocessor, cmp, hardware parallelism, memory-level parallelism, processor architecture, sst




Also published in:  
 June 2009 **SIGARCH Computer Architecture News** Volume 37 Issue 3

- 7 **CAVA: Using checkpoint-assisted value prediction to hide L2 misses**

-  Luis Ceze, Karin Strauss, James Tuck, Josep Torrellas, Jose Renau  
 June 2006 **Transactions on Architecture and Code Optimization (TACO)**  
**Publisher:** ACM  Request Permissions  
 Full text available:  Pdf (646.62 KB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 44, Downloads




Modern superscalar processors often suffer long stalls because of load n problem, we propose hiding L2 misses with Checkpoint-Assisted Value g predicted value is returned ...

**Keywords:** Value prediction, checkpointed processor architectures, me

- 8 **A model to exploit power-performance efficiency in superscalar proc**  
 Omer Khan, Sandip Kundu  
 May 2010 **GLSVLSI '10: Proceedings of the 20th symposium on Great I**  
**Publisher:** ACM  Request Permissions  
 Full text available:  Pdf (770.85 KB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 7, Downloads



Power consumption has become a major cause of concern spanning for Traditionally, improvement in power-performance efficiency of a modern scaling. However, that is no longer ...

**Keywords:** modeling, power


- 9 **Incrementally parallelizing database transactions with thread-level sp**  
 Christopher B. Colohan, Anastassia Ailamaki, J. Gregory Steffan, Todd C. M  
 February 2008 **Transactions on Computer Systems (TOCS)**, Volume 26 is  
**Publisher:** ACM  Request Permissions  
 Full text available:  Pdf (2.82 MB) Additional Information: [full citation](#), [abstract](#)  
**Bibliometrics:** Downloads (6 Weeks): 9, Downloads (12 Months): 159, Downloads

With the advent of chip multiprocessors, exploiting intratransaction pari way of improving transaction performance. However, exploiting intratrans reasons: first, significant ...


**Keywords:** Thread-level speculation, chip-multiprocessing, incrementa

- 10 **Pinot: Speculative Multi-threading Processor Architecture Exploiting Granularities**  
 Taku Ohsawa, Masamichi Takagi, Shoji Kawahara, Satoshi Matsushita  
 November 2005 **MICRO 38: Proceedings of the 38th annual IEEE/ACM Inte**  
**Publisher:** IEEE Computer Society  
 Full text available:  Publisher Site,  Pdf (592.97 KB) Additional Information: [full citation](#)  
**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 48, Downloads

We propose a speculative multi-threading processor architecture called range of granularities without modifying program sources. Since exploit limits of parallelism ...

- 11 **Structure-driven optimizations for amorphous data-parallel programs**  
 Mario Méndez-Lojo, Donald Nguyen, Dimitrios Prountzos, Xin Su, M. Ambe Keshav, Pingali  
 January 2010 **PPoPP '10**: Proceedings of the 15th ACM SIGPLAN symposium on programming

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (559.91 KB)

[Additional Information](#): full citation, abstract


**Bibliometrics:** Downloads (6 Weeks): 37, Downloads (12 Months): 154, Downloads

Irregular algorithms are organized around pointer-based data structure: ubiquitous in applications. Recent work by the Galois project has provided irregular applications based ...

**Keywords:** amorphous data-parallelism, cautious operator implementation, coalescing, one-shot optimization, optimistic parallelization, synchronization

- 12 **POSH: a TLS compiler that exploits program structure**  
 Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau, J March 2006 **PPoPP '06**: Proceedings of the eleventh ACM SIGPLAN symposium on programming

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (157.11 KB)

[Additional Information](#): full citation, abstract

**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 66, Downloads

As multi-core architectures with Thread-Level Speculation (TLS) are becoming focus on TLS compilation. TLS compilers are interesting in that, while the independence of concurrent tasks, ...

**Keywords:** TLS compiler, multi-core architecture, prefetching, profiling

- 13 **A probabilistic pointer analysis for speculative optimizations**  
 Jeff Da Silva, J. Gregory Steffan  
 November 2006 **ASPLOS-XII**: Proceedings of the 12th international conference on programming languages and operating systems

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (260.58 KB)

[Additional Information](#): full citation, abstract

**Bibliometrics:** Downloads (6 Weeks): 14, Downloads (12 Months): 79, Downloads

Pointer analysis is a critical compiler analysis used to disambiguate the use of pointers and pointer-based data structures. A conventional pointer analysis, at any program ...

**Keywords:** dependence analysis, pointer analysis, speculative optimization


Also published in:

October 2006 **SIGARCH Computer Architecture News** Volume 34 Issue 5




October 2006 **SIGOPS Operating Systems Review** Volume 40 Issue 5

November 2006 SIGPLAN Notices

Volume 41 Issue 11



- 14 [Decoupled Software Pipelining with the Synchronization Array](#)  
 Ram Rangan, Neil Vachharajani, Manish Vachharajani, David I. August  
 September 2004 **PACT '04: Proceedings of the 13th International Conference on Techniques**  
**Publisher:** IEEE Computer Society  
 Full text available:  [Pdf](#) (311.44 KB) Additional Information: full citation, abstract  
**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 62, Downloads

Despite the success of instruction-level parallelism (ILP) optimizations in microprocessors, certain codes remain elusive. In particular, codes containing traversal loops have been largely ...




- 15 [On approximating the ideal random access machine by physical machines](#)  
 Gianfranco Bilardi, Kattamuri Ekanadham, Pratap Pattanaik  
 August 2009 **Journal of the ACM (JACM)**, Volume 56 Issue 5  
**Publisher:** ACM  Request Permissions  
 Full text available:  [Pdf](#) (834.87 KB) Additional Information: full citation, abstract  
**Bibliometrics:** Downloads (6 Weeks): 11, Downloads (12 Months): 223, Downloads

The capability of the *Random Access Machine* (RAM) to execute any instruction set to fundamental physical constraints on the minimum size of devices and explores how ...

**Keywords:** Physical constraints on machines, pipelined hierarchical machines

- 16 [ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions](#)  
 Smruti R. Sarangi, Wei Liu, Josep Torrellas, Yuanyuan Zhou  
 November 2005 **MICRO 38: Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture**  
**Publisher:** IEEE Computer Society  
 Full text available:  [Publisher Site](#),  [Pdf](#) (428.43 KB) Additional Information: full citation, abstract  
**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 21, Downloads


As more data value speculation mechanisms are being proposed to speed up execution on the critical processor structures that must buffer the state of the speculative instructions, it is important to understand the impact of the speculative instructions on the processor ...

- 17 [Inferential queueing and speculative push for reducing critical communication latencies](#)  
 Ravi Rajwar, Alain Kagi, James R. Goodman  
 June 2003 **ICS '03: Proceedings of the 17th annual international conference on Supercomputing**  
**Publisher:** ACM  Request Permissions  
 Full text available:  [Pdf](#) (568.93 KB) Additional Information: full citation, abstract  
**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 26, Downloads

Communication latencies within critical sections constitute a major bottleneck in many parallel workloads. In this paper, we argue for the use of Inferentially Queued Locks (IQLs) for synchronization but also ...

**Keywords:** data forwarding, inferential queueing, synchronization

18 [Extending concurrency of transactional memory programs by using \](#)

 Salil Mohan Pant, Gregory T. Byrd

May 2009

**CF '09:** Proceedings of the 6th ACM conference on Computing

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (877.06 KB)


Additional Information: [full citation](#), [abst](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 118, Downlo

Transactional Memory (TM) is an optimistic speculative synchronization region of code marked as a transaction by the programmer. TM avoids i based synchronization and ...

**Keywords:** logtm, transactional memory, value prediction

19 [An integrated hardware-software approach to flexible transactional n](#)

 Arvindh Shriraman, Michael F. Spear, Hemayet Hossain, Virendra J. Marat

June 2007

**ISCA '07:** Proceedings of the 34th annual international symp

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (637.98 KB)

Additional Information: [full citation](#), [abst](#)

**Bibliometrics:** Downloads (6 Weeks): 21, Downloads (12 Months): 147, Downl


There has been considerable recent interest in both hardware and software an intermediate approach, in which hardware serves to accelerate a TM i software. Specifically, we ...

**Keywords:** RSTM, cache coherence, multiprocessors, transactional me

Also published in:

June 2007 **SIGARCH Computer Architecture News** Volume 35 Issue 2

20 [Fire-and-Forget: Load/Store Scheduling with No Store Queue at All](#)

 Samantika Subramaniam, Gabriel H. Loh

December 2006

**MICRO 39:** Proceedings of the 39th Annual IEEE/ACM Inte

**Publisher:** IEEE Computer Society

Full text available:  Pdf (357.14 KB)

Additional Information: [full citation](#), [abst](#)

**Bibliometrics:** Downloads (6 Weeks): 9, Downloads (12 Months): 68, Downloa

Modern processors use CAM-based load and store queues (LQ/SQ) to su store-to-load forwarding. However, the LQ and SQ scale poorly for the s processors. Past research has ...

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 Marcelo Cintra, Diego R. Llanos  
 June 2003 **PPoPP '03: Proceedings of the ninth ACM SIGPLAN symposi**  
 programming

**Publisher:** ACM [Request Permissions](#)

Full text available: Pdf (330.64 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 101, Downlo

 With speculative parallelization, code sections that cannot be fully analy  
 parallel. Hardware schemes are fast but expensive and require modifica  
 Software schemes ...

**Keywords:** speculative parallelization, thread-level speculation

Also published in:

 October 2003 **SIGPLAN Notices** Volume 38 Issue 10

- 2 **Inferential queueing and speculative push for reducing critical comm**  
 Ravi Rajwar, Alain Kägi, James R. Goodman  
 June 2003 **ICS '03: Proceedings of the 17th annual international confer**

**Publisher:** ACM [Request Permissions](#)

Full text available: Pdf (568.93 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 26, Downloa

 Communication latencies within critical sections constitute a major bottl  
 workloads. In this paper, we argue for the use of Inferentially Queued L  
 synchronization but also ...

**Keywords:** data forwarding, inferential queueing, synchronization

- 3 **Exploiting multiple functionality for nano-scale reconfigurable system**  
 Paul Beckett  
 April 2003 **GLSVLSI '03: Proceedings of the 13th ACM Great Lakes syr**

**Publisher:** ACM [Request Permissions](#)



Full text available:  Pdf (197.22 KB)

Additional Information: full citation, at

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It is likely that it will become increasingly difficult to manufacture the cc characterise current reconfigurable logic systems. As a result, these sys of largely ...


**Keywords:** RTD, carbon nanotube, chalcogenide, double gate transisto nanoelectronics, nanotechnology, reconfigurable systems, resonant tuni

#### 4 Load and store reuse using register file contents



Soner Onder, Rajiv Gupta

June 2001

**ICS '01:** Proceedings of the 15th international conference on**Publisher:** ACM Full text available:  Pdf (251.51 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 21, Download


The detection of opportunities for value reuse optimizations in memory associated with these operations to be available. Although the values ar their ...

#### 5 Reference idempotency analysis: a framework for optimizing specul



Seon Wook Kim, Chong-ilang Ooi, Rudolf Eigenmann, Babak Falsafi, T. N. A

July 2001

**PPoPP '01:** Proceedings of the eighth ACM SIGPLAN sympos programming**Publisher:** ACM Full text available:  Pdf (329.79 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 20, Download

Recent proposals for multithreaded architectures allow threads with unk parallel. These architectures use hardware speculative storage to buffer roll ...

Also published in:

July 2001 **SIGPLAN Notices** Volume 36 Issue 7

#### 6 A general compiler framework for speculative multithreading



Anasua Bhowmik, Manoj Franklin

August 2002

**SPAA '02:** Proceedings of the fourteenth annual ACM sympo**Publisher:** ACM Full text available:  Pdf (131.41 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 90, Download

Speculative multithreading (SpMT) promises to be an effective mechani tend to use irregular data structures with pointers and have complex fic obtaining ...

**Keywords:** TLP compiler, control dependence, data dependence, parall



thread formation, thread-level parallelism (TLP)

### 7 Register Synthesis for Speculative Computation

Dirk Herrmann, Rolf Ernst

March 1997 **EDTC '97**: Proceedings of the 1997 European conference on

**Publisher**: IEEE Computer Society

Full text available:  [Publisher Site](#) ,  Pdf (639.76 KB) Additional Information: full citation, at

**Bibliometrics**: Downloads (6 Weeks): 0, Downloads (12 Months): 1, Download

Speculative computation and branch prediction have been used in high-level synthesis. Recently, it has also been applied to high-level synthesis where a priori even higher performance ...

**Keywords**: high-level-synthesis, register synthesis, life time analysis, s

### 8 Containers on the Parallelization of General-Purpose Java Programs

Peng Wu, David Padua

October 1999 **PACT '99**: Proceedings of the 1999 International Conference on Parallel Architectures and Techniques

**Publisher**: IEEE Computer Society


Full text available:  [Publisher Site](#) Additional Information: full citation, at

**Bibliometrics**: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Download

Automatic parallelization of general-purpose programs is still not possible for complex control-flows. One promising strategy is thread-level parallelism which alleviates the ...

**Keywords**: compiler parallelization, dependence test, Java parallelization

### 9 Parallel multiplication: a case study in parallel programming

 C. K. Yuen, M. D. Feng

March 1994 **SIGPLAN Notices** , Volume 29 Issue 3

**Publisher**: ACM

Full text available:  Pdf (437.48 KB) Additional Information: full citation, at

**Bibliometrics**: Downloads (6 Weeks): 2, Downloads (12 Months): 29, Download

Six versions of a parallel program for multiplication are presented, and they illustrate the bottom up and top down methods of program structure development and processing in ...

### 10 Performance modelling of speculative prefetching for compound requests

 N. J. Tuah, M. J. Kumar, S. Venkatesh

August 2000 **WOWMOM '00**: Proceedings of the 3rd ACM international workshop on Web-Oriented Web Modeling and Management

**Publisher**: ACM 

Full text available:  Pdf (817.34 KB) Additional Information: full citation, at



**Bibliometrics**: Downloads (6 Weeks): 1, Downloads (12 Months): 8, Download

To improve the accuracy of access prediction, a prefetcher for web browsing is proposed. It uses a performance model to predict the next page to be accessed. The model is trained using a set of web browsing traces. The prefetcher is implemented in a web browser. It improves the accuracy of access prediction, and thus reduces the time to fetch the next page. The prefetcher is evaluated using a set of web browsing traces. It shows that the prefetcher improves the accuracy of access prediction, and thus reduces the time to fetch the next page. The prefetcher is implemented in a web browser. It improves the accuracy of access prediction, and thus reduces the time to fetch the next page. The prefetcher is evaluated using a set of web browsing traces. It shows that the prefetcher improves the accuracy of access prediction, and thus reduces the time to fetch the next page.

a compound. By this term we mean that a user request for a single web multimedia items. ...

**Keywords:** Web, caching, compound requests, speculative prefetching



#### 11 Pointer cache assisted prefetching

Jamison Collins, Suleyman Sair, Brad Calder, Dean M. Tullsen  
November 2002 **MICRO 35**: Proceedings of the 35th annual ACM/IEEE inter  
**Publisher:** IEEE Computer Society Press  
Full text available:  [Publisher Site](#),  [Pdf \(1.21 MB\)](#) Additional Information: [full citation](#),

**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 31, Download

Data prefetching effectively reduces the negative effects of long load lat  
Hardware prefetchers employ hardware structures to predict future mem  
Thread-based prefetchers ...

#### 12 A fill-unit approach to multiple instruction issue



 Manoj Franklin, Mark Smotherman  
November 1994 **MICRO 27**: Proceedings of the 27th annual international sym  
**Publisher:** ACM  
Full text available:  [Pdf \(992.94 KB\)](#) Additional Information: [full citation](#), at

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 19, Download

Multiple issue of instructions occurs in superscalar and VLIW machines.  
design, which combines the advantages of code compatibility as in super  
checking logic ...

**Keywords:** VLIW, instruction-level parallelism, multiple operation issue

#### 13 Streamlining inter-operation memory communication via data depend

Andreas Moshovos, Gurindar S. Sohi  
December 1997 **MICRO 30**: Proceedings of the 30th annual ACM/IEEE inter  
**Publisher:** IEEE Computer Society  
Full text available:  [Publisher Site](#),  [Pdf \(1.73 MB\)](#) Additional Information: [full citation](#),

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 23, Download


We revisit memory hierarchy design viewing memory as an inter-operat  
to the development of novel methods of performing inter-operation mem  
prediction to identify ...

**Keywords:** DEF-store-load-USE chains, address calculation, address di  
access, data cache bandwidth requirements, data dependence prediction  
communication, memory architecture, memory dependences, memory l  
value cache

#### 14 Dynamically assembled documentation

 Michael Priestley  
October 1999 **SIGDOC '99**: Proceedings of the 17th annual international co

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (598.27 KB)


Additional Information: [full citation](#), at

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 9, Download

As online information becomes more comprehensive in its scope, the sh  
Information needs to be both browsable and searchable, and both need  
approach (such as SGML ...

**Keywords:** dynamic documentation, reference documentation, structur


# 15 A retrospective on the Dorado, a high-performance personal comput

 Kenneth A. Pier

June 1983

**ISCA '83:** Proceedings of the 10th annual international symp

**Publisher:** ACM

Full text available:  Pdf (2.01 MB)

Additional Information: [full citation](#), at

**Bibliometrics:** Downloads (6 Weeks): 1, Downloads (12 Months): 30, Downloa

In late 1975, members of the Xerox Palo Alto Research Center embarke  
successor to the Alto personal minicomputer, in use since 1973. After fo  
Dorado, was in use within ...

Also published in:

June 1983 **SIGARCH Computer Architecture News** Volume 11 Issue 3


# 16 Architectural support for scalable speculative parallelization in share

 Marcelo Cintra, José F. Martínez, Josep Torrellas

June 2000

**ISCA '00:** Proceedings of the 27th annual international symp

**Publisher:** ACM

Full text available:  Pdf (253.29 KB)

Additional Information: [full citation](#), at


**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 76, Downloa

Speculative parallelization aggressively executes in parallel codes that c  
proposals of hardware schemes have mostly focused on single-chip mul  
necessarily limited ...

Also published in:

May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

# 17 A compiler framework for speculative analysis and optimizations

 Jin Lin, Tong Chen, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin

June 2003

**PLDI '03:** Proceedings of the ACM SIGPLAN 2003 conference  
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**Publisher:** ACM  [Request Permissions](#)

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Additional Information: [full citation](#), at

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Speculative execution, such as control speculation and data speculation  
performance. Using edge/path profile information or simple heuristic rul  
incorporate and exploit ...

**Keywords:** data speculation, partial redundancy elimination, register p update


Also published in:

May 2003 **SIGPLAN Notices** Volume 38 Issue 5

# 18 The Jrpm system for dynamically parallelizing Java programs

 Michael K. Chen, Kunle Olukotun  
June 2003

**ISCA '03: Proceedings of the 30th annual international symposium on**  
**Publisher:** ACM

Full text available:  Pdf (320.42 KB)

Additional Information: full citation, at


**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 73, Downloa

We describe the Java runtime parallelizing machine (Jrpm), a complete automatically. Jrpm is based on a chip multiprocessor (CMP) with thread sharing and communication ...

Also published in:



May 2003 **SIGARCH Computer Architecture News** Volume 31 Issue 2

# 19 Computing curricula 2001

 CORPORATE The Joint Task Force on Computing Curricula  
September 2001


**Journal on Educational Resources in Computing (JER**

**Publisher:** ACM  Request Permissions

Full text available:  Html (2.78 KB),  Pdf (613.63 KB) Additional Information: full citati

**Bibliometrics:** Downloads (6 Weeks): 91, Downloads (12 Months): 1091, Dowr

# 20 An evaluation of speculative instruction execution on simultaneous n

 Steven Swanson, Luke K. McDowell, Michael M. Swift, Susan J. Eggers, Hei  
August 2003

**Transactions on Computer Systems (TOCS)**, Volume 21 Iss

**Publisher:** ACM  Request Permissions

Full text available:  Pdf (578.85 KB)

Additional Information: full citation, at

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 44, Downloa

Modern superscalar processors rely heavily on speculative execution for show that on a 6-issue superscalar, 93&percent; of committed instruction speculation, processor ...

**Keywords:** Instruction-level parallelism, multiprocessors, multithreadin thread-level parallelism

Result pag

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**1** Process migration

 Dejan S. Milošević, Fred Douglass, Yves Paindaveine, Richard Wheeler, Songni  
 September 2000 **Computing Surveys (CSUR)**, Volume 32 Issue 3

**Publisher:** ACM Request Permissions

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Process migration is the act of transferring a process between two machine system administration, and data access locality. Despite these goals and

**Keywords:** distributed operating systems, distributed systems, load distribution

**2** Principled design of the modern Web architecture

 Roy T. Fielding, Richard N. Taylor  
 May 2002

**Transactions on Internet Technology (TOIT)**, Volume 2

**Publisher:** ACM Request Permissions

Full text available: Pdf (335.47 KB)

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The World Wide Web has succeeded in large part because its software is a distributed hypermedia application. The modern Web architecture emphasizes

**Keywords:** Network-based applications, REST, World Wide Web

**3** Extended ephemeral logging: log storage management for applications

John S. Keen, William J. Dally

 March 1997 **Transactions on Database Systems (TODS)**, Volume 22 Issue

**Publisher:** ACM Request Permissions

Full text available: Pdf (566.34 KB)

Additional Information: full citation, reference

**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 36, Downloads

**Keywords:** OLTP, disk management, logging, long transactions




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-  **The design of an acquisitional query processor for sensor networks**  
 Samuel Madden, Michael J. Franklin, Joseph M. Hellerstein, Wei Hong  
 June 2003 **SIGMOD '03: Proceedings of the 2003 ACM SIGMOD inter**  
**Publisher:** ACM  [Request Permissions](#)  
 Full text available:  Pdf (485.52 KB) [Additional Information: full cit](#)  
**Bibliometrics:** Downloads (6 Weeks): 14, Downloads (12 Months): 203, Downl

We discuss the design of an acquisitional query processor for data colle where, when, and how often data is physically acquired (*sampled*) and i

- 5 **Principled design of the modern Web architecture**  
 Roy T. Fielding, Richard N. Taylor  
 June 2000 **ICSE '00: Proceedings of the 22nd international conferenc**  
**Publisher:** ACM  
 Full text available:  Pdf (217.34 KB) [Additional Information: full cit](#)  
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The World Wide Web has succeeded in large part because its software a distributed hypermedia system. The modern Web architecture emphasiz

**Keywords:** WWW, software architectural style, software architecture

- 6 **Disconnection modes for mobile databases**  
 Joanne Holliday, Divyakant Agrawal, Amr El Abbadi  
 July 2002 **Wireless Networks**, Volume 8 Issue 4  
**Publisher:** Kluwer Academic Publishers  
 Full text available:  Pdf (198.57 KB) [Additional Information: full cit](#)  
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As mobility permeates into todays computing and communication arena mobile technologies. Traditional database applications and information s

**Keywords:** data consistency, databases, disconnected operation, mobil

- 7 **A dynamic grouping technique for ink and audio notes**  
 Patrick Chiu, Lynn Wilcox  
 November 1998 **UIST '98: Proceedings of the 11th annual ACM symposium**  
**Publisher:** ACM  [Request Permissions](#)  
 Full text available:  Pdf (98.41 KB) [Additional Information: full cit](#)  
**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 17, Downloa

**Keywords:** audio, clustering multimedia, emergent structure, freeform marking, note-taking

- 8 **Difficulties in simulating the internet**  
 Sally Floyd, Vern Paxson  
 August 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume  
**Publisher:** IEEE Press


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Simulating how the global Internet behaves is an immensely challenging change. The heterogeneity ranges from the individual links that carry th

**Keywords:** Internet, modeling, simulation**9 Formal verification of standards for distance vector routing protocols**

 Karthikeyan Bhargavan, Davor Obradovic, Carl A. Gunter  
July 2002 **Journal of the ACM (JACM)**, Volume 49 Issue 4


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We show how to use an interactive theorem prover, HOL, together with routing protocols. We do three case studies: correctness of the RIP stan

**Keywords:** AODV, Formal verification, HOL, RIP, SPIN, distance vector standards, routing protocols**10 A practical comparison between Java and Ada in implementing a re**

 Eric Potratz  
December 2003 **SigAda '03: Proceedings of the 2003 annual ACM SIGAda reliable software for real-time & distributed systems using**

**Publisher:** ACM  Request PermissionsFull text available:  Pdf (259.58 KB)

Additional Information: full cit

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This paper presents a student's observations from an undergraduate re: a real-time embedded system that was originally implemented in a univ

**Keywords:** Ada, Java, concurrency, conditional synchronization, driver programming, package elaboration, performance, priority inversion, rea

Also published in:

March 2004 **SIGAda Ada Letters** Volume XXIV Issue 1**11 On-Demand Grid Application Tuning and Debugging with the NetLog**

Dan Gunter, Brian L. Tierney, Craig E. Tull, Vibha Virmani


November 2003 **GRID '03: Proceedings of the 4th International Workshop****Publisher:** IEEE Computer SocietyFull text available:  Pdf (220.36 KB)

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Typical Grid computing scenarios involve manydistributed hardware and more likely it is that oneof them may fail. In order for Grid computing to



- 12 [An alternating offers bargaining model for computationally limited agents](#)  
 Kate Larson, Tuomas Sandholm  
 July 2002 **AAMAS '02: Proceedings of the first international joint conference on Autonomous Agents and Multi-Agent Systems**

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An alternating offers bargaining model for computationally limited agents restrict them from determining an optimal solution. As the agents compute

- 13 [Quantifying and Improving the Availability of High-Performance Clusters](#)  
 Kiran Nagaraja, Neeraj Krishnan, Ricardo Bianchini, Richard P. Martin, Thiru  
 November 2003 **SC '03: Proceedings of the 2003 ACM/IEEE conference on Supercomputing**


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Cluster-based servers can substantially increase performance when nodes show that cooperation results in a substantial availability loss, in the absence of


- 14 [Side views: persistent, on-demand previews for open-ended tasks](#)  
 Michael Terry, Elizabeth D. Mynatt  
 October 2002 **UIST '02: Proceedings of the 15th annual ACM symposium on User Interface Software Technology**

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Mov (300.00 bytes),  Pdf (479.12 KB),  Wmv (300.00 bytes) [View](#)

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We introduce Side Views, a user interface mechanism that provides one designed to explicitly support the practices and needs of expert use

- 15 [Interruptible rendering](#)  
 Cliff Woolley, David Luebke, Benjamin Watson, Abhinav Dayal  
 April 2003 **I3D '03: Proceedings of the 2003 symposium on Interactive 3D Graphics**

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Interruptible rendering is a novel approach to the fidelity-versus-performance rendering unifies spatial error caused by rendering coarse approximations

**Keywords:** level of detail, mesh simplification, perceptually motivated

- 16 [Experience report: exploiting advanced database optimization features](#)  
 Bernhard Zeller, Alfons Kemper  
 August 2002 **VLDB '02: Proceedings of the 28th international conference on Very Large Data Bases**

**Publisher:** VLDB Endowment

Full text available:  Pdf (169.88 KB)

Additional Information: [full cit](#)

**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 54, Downloads

The database volumes of enterprise resource planning (ERP) systems lil already reached a size of several Terabytes. OLTP (Online Transaction P


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Ricki G. Ingalls

December 2001

**WSC '01:** Proceedings of the 33nd conference on Winter s

**Publisher:** IEEE Computer Society

Full text available:  Pdf (408.79 KB)

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**WSC '02:** Proceedings of the 34th conference on Winter si

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May 1995

**CHI '95:** Proceedings of the SIGCHI conference on Human fac


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**Protein structure prediction by a data-level parallel algorithm**

Zhang, X.; Waltz, D.; Mesirov, J. P.;  
Supercomputing, 1989. Supercomputing '89. Proceedings of  
the 1989 ACM/IEEE Conference on  
Digital Object Identifier: 10.1145/76263.76286  
Publication Year: 1989 , Page(s): 215 - 223

**IEEE CONFERENCES****Designing programming languages for analyzability:  
a fresh look at pointer data structures**

Hendren, L.J.; Gao, G.R.;  
Computer Languages, 1992., Proceedings of the 1992  
International Conference on  
Digital Object Identifier: 10.1109/ICCL.1992.185488  
Publication Year: 1992 , Page(s): 242 - 251

**IEEE CONFERENCES****Efficient management of speculative data in  
hardware transactional memory systems**

Waliullah, M.M.; Stenstrom, P.;  
Embedded Computer Systems: Architectures, Modeling, and  
Simulation, 2008. SAMOS 2008. International Conference on  
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Mahl, R.;  
Computers, IEEE Transactions on  
Volume: C-21 , Issue: 1  
Publication Year: 1972 , Page(s): 1 - 4

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Shih-Chang Lai;  
Computer Design, 2003. Proceedings. 21st International  
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Digital Object Identifier: 10.1109/ICCD.2003.1240909  
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Leventhal, S.; Franklin, M.;  
Computer Design, 2006. ICCD 2006. International Conference  
on  
Digital Object Identifier: 10.1109/ICCD.2006.4380808  
Publication Year: 2006 , Page(s): 148 - 154

**IEEE CONFERENCES****Querying XML documents made easy: nearest concept queries**

Schmidt, A.; Kersten, M.; Windhouwer, M.;  
Data Engineering, 2001. Proceedings. 17th International  
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Digital Object Identifier: 10.1109/ICDE.2001.914844  
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**IEEE CONFERENCES****Modeling load address behaviour through recurrences**

Ramos, L.; Ibanez, P.; Vinals, V.; Llaveria, J.M.;  
Performance Analysis of Systems and Software, 2000. ISPASS.  
2000 IEEE International Symposium on  
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Publication Year: 2000 , Page(s): 101 - 108

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Yuen, C.K.; Feng, M.D.; Yee, J.J.;  
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Digital Object Identifier: 10.1109/ICCI.1993.315367  
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**Speculative lock reordering: optimistic out-of-order execution of critical sections**

Rundberg, P.; Stenstrom, P.;  
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Digital Object Identifier: 10.1109/IPDPS.2003.1213086  
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**Speculative search: An efficient search algorithm for limited memory**

Gooley, M.M.; Wah, B.W.;  
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1993 International Joint Conference on  
Volume: 3  
Digital Object Identifier: 10.1109/IJCNN.1993.714218  
Publication Year: 1993 , Page(s): 2441 - 2447 vol.3

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**The SPARAMAT approach to automatic comprehension of sparse matrix computations**

Kessler, C.W.; Smith, C.H.;  
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Digital Object Identifier: 10.1109/WPC.1999.777759  
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Refice, A.; Bovenga, F.; Nutricato, R.; Chiaradia, M.T.;  
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**IEEE CONFERENCES****Pointer cache assisted prefetching**

Collins, J.; Sair, S.; Calder, B.; Tullsen, D.M.;  
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Digital Object Identifier: 10.1109/MICRO.2002.1176239  
Publication Year: 2002 , Page(s): 62 - 73

**IEEE CONFERENCES****LATEX human motion planning based on recursive dynamics and optimal control techniques**

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Computer Graphics International, 2000. Proceedings  
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Kulkarni, M.; Pingali, K.;  
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Digital Object Identifier: 10.1109/IPDPS.2007.370491  
Publication Year: 2007 , Page(s): 1 - 7

**IEEE CONFERENCES****B<sup>+</sup>-tree indexes with hybrid row identifiers in Oracle8i**

Eugene Inseok Chong; Souripriya Das; Yalamanchi, A.;  
Jagannath, M.; Freilwald, C.; Srinivasan, J.; Anh-Tuan Tran;  
Krishnan, R.;  
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Digital Object Identifier: 10.1109/ICDE.2001.914846  
Publication Year: 2001 , Page(s): 341 - 348

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Peng Wu; Padua, D.;  
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Publication Year: 1999 , Page(s): 84 - 90

**IEEE CONFERENCES****Fire-and-Forget: Load/Store Scheduling with No Store Queue at All**

Samantika Subramaniam; Gabriel H. Loh;  
Microarchitecture, 2006. MICRO-39. 39th Annual IEEE/ACM International Symposium on  
Digital Object Identifier: 10.1109/MICRO.2006.26  
Publication Year: 2006 , Page(s): 273 - 284

**IEEE CONFERENCES****Speculative processing mechanisms in a parallel Lisp machine: BIDDLE**

Yee, J.J.; Feng, M.D.; Yuen, C.K.;  
System Sciences, 1993, Proceeding of the Twenty-Sixth Hawaii International Conference on  
Volume: 1  
Digital Object Identifier: 10.1109/HICSS.1993.270619  
Publication Year: 1993 , Page(s): 457 - 465 vol.1

**IEEE CONFERENCES****Multiple zone inverse diffusion solver for silicon processing**

Wang, Y.S.; Mastrangelo, C.H.;  
Simulation of Semiconductor Processes and Devices, 1997. SISPAD '97., 1997 International Conference on  
Digital Object Identifier: 10.1109/SISPAD.1997.621382  
Publication Year: 1997 , Page(s): 241 - 244

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Figueiredo, R.J.; Fortes, J.A.B.;  
Parallel Processing, International Conference on, 2001.  
Digital Object Identifier: 10.1109/ICPP.2001.952065  
Publication Year: 2001 , Page(s): 214 - 224

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Koczy, L.T.; Ballagi, A.;  
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Bhowmik, A.; Franklin, M.;

Parallel and Distributed Systems, IEEE Transactions on  
Volume: 15 , Issue: 8

Digital Object Identifier: 10.1109/TPDS.2004.26

Publication Year: 2004 , Page(s): 713 - 724

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**Future Technologies for Medical Applications**

Marsh, A.; Marsh, A.; Marsh, A.; Marsh, A.; Akay, M.; Akay, M.; Akay, M.; Akay, M.;  
Information Technologies in Medicine, Medical Simulation and Education

Digital Object Identifier: 10.1002/0471216690.ch9

Publication Year: 2001 , Page(s): 219 - 236

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Pajuelo, A.; Gonzalez, A.; Valero, M.;  
Computer Architecture, 2002. Proceedings. 29th Annual International Symposium on  
Digital Object Identifier: 10.1109/ISCA.2002.1003585  
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**IEEE CONFERENCES****Blind de-mixing with unknown sources**

Szu, H.; Hsu, C.;  
Neural Networks, 1997., International Conference on  
Volume: 4  
Digital Object Identifier: 10.1109/ICNN.1997.614686  
Publication Year: 1997 , Page(s): 2513 - 2518 vol.4

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Kaxiras, S.; Young, C.;  
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**IEEE CONFERENCES**

**Dispersion properties of periodic grounded structures via equivalent network synthesis**

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Publication Year: 2003 , Page(s): 493 - 496 vol.1

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**Future Technologies for Medical Applications**

Marsh, A.; Marsh, A.; Marsh, A.; Marsh, A.; Akay, M.; Akay, M.; Akay, M.; Akay, M.;  
Information Technologies in Medicine, Medical Simulation and Education  
Digital Object Identifier: 10.1002/0471216690.ch9  
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Qiang Chen; Zhi-Yuan Wu; Ly, T.; Gupta, M.; Wason, V.; Jung-Suk Goo; Thuruthiyil, C.; Radwin, M.; Subba, N.; Chiney, P.; Suryagandh, S.; Icel, A.B.;  
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**Dispersion properties of periodic grounded structures via equivalent network synthesis**

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Computer Vision and Pattern Recognition, 2008. CVPR 2008.  
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**ADMiRe: an algebraic data mining approach to system performance analysis**

Jiang, N.; Villafane, R.; Hua, K.A.; Sawant, A.; Prabhakara, A.;  
Knowledge and Data Engineering, IEEE Transactions on  
Volume: 17 , Issue: 7  
Digital Object Identifier: 10.1109/TKDE.2005.103  
Publication Year: 2005 , Page(s): 888 - 901

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**Discovering the Rules in a Poker Player's Mind Based on the Association Rule Mining**

Mehrabi, A.; Haghighat, A.T.;  
Computer Technology and Development, 2009. ICCTD '09.  
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Adda, M.; Valtchev, P.; Missaoui, R.; Djeraba, C.;  
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Volume: 11 , Issue: 4  
Digital Object Identifier: 10.1109/MIC.2007.93

Publication Year: 2007 , Page(s): 45 - 52

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**Gamma ray burst afterglow studies in Turkey**

Kacar, Y.; Ozel, M.E.; Olutas, M.; Guver, T.; Kiziloglu, U.;  
Recent Advances in Space Technologies, 2005. RAST 2005.  
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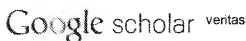
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